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Lossy & Lossless Capacitance Multipliers: A Series of Realization Using VDTAs & Single Grounded Capacitor

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Abstract

The article presents new realizations of capacitance multiplier circuits, employing two voltage differencing transconductance amplifiers (VDTAs) and one capacitor without any passive resistors. The equivalent capacitance value of the proposed capacitance simulators can be achieved electronically by regulating the DC bias currents of VDTAs. All the proposed realizations do not require any critical component matching conditions. The lossless floating negative capacitor multiplier (NCM) circuit is studied in detail. The capacitive cancellation scheme and a quadrature sinusoidal oscillator circuit are included to demonstrate the effectiveness of the circuit. The effect of the VDTAs non-idealities and parasitic on the realized circuits is analysed. SPICE simulation results using TSMC 0.18 µm CMOS technology parameters are presented to reflect the workability of the proposed NCM. The simulation results are in excellent agreement with the theoretical calculation. In addition to these, a comparison with the previously reported circuits is summarized to confirm the superiority of the recommended NCM.

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Keywords: Capacitance multiplier, parasitic capacitance cancellation, electronic control, multiplication factor, voltage differencing transconductance amplifier

1. Introduction

Large-valued capacitors are key components in analog ICs employed in analog signal processing applications like continuous time filters, sensors, phase-locked loops, sample-and-hold data systems and oscillators. However, direct realization of the large-value capacitors is difficult in integrated circuit technology because a large silicon area is needed on the chip. To overcome these limitations, the capacitance multiplier (CM) technique is introduced.

A number of capacitance multiplier circuits have been previously reported using different active blocks, such as, current follower transconductance amplifier (CFTA) (Özer, 2021), second generation voltage conveyor (VCII) (Stornelli et al., 2021), current differencing transconductance amplifier (CDTA) (Biolek et al., 2019), voltage difference current conveyors (VDCC) (Gupta et al., 2019), current operational amplifier (COA) and current controlled current conveyor trans-conductance amplifier (CCCCTA) (Siripruchyanun et al., 2019), voltage differencing gain amplifier (VDGA) (Tangsrirat et al., 2019), third-generation current conveyor transconductance amplifier (CCIIITA) (Singh et al., 2020), operational transresistance amplifier (OTRA) (Nagar & Paul, 2021), current feedback operational amplifier (CFOA) (Dogan & Yuce, 2020; Özer et al., 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020) operational transconductance amplifier (OTA) (Singh et al., 2020; Jaikla & Siripruchyanan, 2006; Rivera-Escobar et al., 2013; Kamath, 2018; Kamat et al., 2011; Al-Absi et al., 2019; Al-Absi & Abulema'atti, 2019), second generation current conveyors (CCII) (Al-Absi et al., 2019; Al-Absi & Abulema'atti, 2019), negative-type second-generation current conveyor (CCII-) and an inverting second generation current conveyor (ICCII) (Yesil et al., 2017), etc. Some of the drawbacks of the former work can be summarized as:

- Use of more than two active blocks (Nagar & Paul, 2021; Abuelma'atti & Dhar, 2016; Singh et al., 2020; Jaikla & Siripruchyanan, 2006; Rivera-Escobar et al., 2013; Kamat et al., 2011; Al-Absi et al., 2019).
- Requirement of resistances (Özer, 2021; Stornelli, 2021; Biolek, 2019; Gupta, 2019; Nagar & Paul, 2021; Dogan & Yuce, 2020; Özer et al., 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020; Al-Absi & Abulema'atti, 2019; Yesil et al., 2017).
- Impossible to tune electronically (Stornelli, 2021; Biolek, 2019; Nagar & Paul, 2021; Dogan & Yuce, 2020; Özer et al., 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Abuelma'atti, 2012; Singh et al., 2020; Yesil et al., 2017).
- Comparatively large supply voltage is required (Stornelli et al., 2021; Biolek, 2019; Siripruchyanun et al., 2019; Tangsrirat et al., 2019; Singh et al., 2020; Dogan & Yuce, 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Singh et al., 2020; Jaikla & Siripruchyanan, 2006; Rivera-Escobar et al., 2013; Kamat et al., 2011; Tangsrirat & Unhavanich, 2016).
- Used capacitors are not grounded (Özer, 2021; Stornelli et al., 2021; Biolek, 2019; Tangsrirat et al., 2019; Nagar & Paul, 2021; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020; Rivera-Escobar et al., 2013; Al-Absi et al., 2019).
- Used mixed active building blocks (Biolek, 2019; Siripruchyanun et al., 2019; Singh et al., 2020; Al-Absi et al., 2019; Al-Absi & Abulema'atti, 2019).

A positive capacitance multiplier circuit using two VDTAs and one grounded capacitor is proposed in (Tangsrirat & Unhavanich, 2014). The topology of (Tangsrirat & Unhavanich, 2014) becomes our topic of contemplation. By making minor changes to this configuration, various lossy and lossless capacitance multiplier circuits can be realized.

In this paper, the major intention is, therefore, to propose a new catalog of capacitance multipliers (CMs) using only two VDTAs and one grounded capacitor. The configurations proposed in the catalog can emulate lossy and lossless CM. The proposed lossless negative CM has been studied in detail. It is worth mentioning here that negative capacitances find a wide range of applications in analog building blocks. It can be used in cancelling stray/parasitic capacitances, in designing of sinusoidal oscillators, in passive vibration damping systems, and in the bandwidth extension of a CMOS amplifier (Abuelma'atti et al., 2017). There is no need for passive element matching conditions. The multiplication factor can be adjusted by the VDTA's bias current, allows it to be electronically tunable. Necessary simulation results have been carried out with the PSPICE program using 0.18 µm TSMC CMOS technology parameters. Application for voltage mode quadrature sinusoidal oscillator and capacitance cancellation circuit are included to reveal the functionality of the circuit. Monte Carlo analysis has been performed to test the robustness of the reported circuit. Moreover, the comparison of the proposed CM with the previously reported CM circuits is also presented.

This study has been divided as follows: The introduction is presented in Section 1, and voltage differencing transconductance amplifier (VDTAs) is introduced in Section 2. Section 3 describes the configurations of the proposed capacitance multipliers (CMs). The non-ideal and parasitic analysis of the proposed configurations are investigated in Sections 4 & Section 5, respectively. Section 6 brings the applications of the reported capacitance multipliers. After that, the results are presented in Section 7 followed by Section 8 where the comparisons of the proposed CM with the previous publication are discussed. Finally, the study is concluded in Section 9.

2. Basic concept of VDTAs

VDTAs is an alternative versatile active building block. The VDTAs symbol and its inner block diagram are illustrated in Figure 1. In VDTAs, P and N are the high impedance voltage input terminals whereas Z, X+ and X− are the high impedance current output terminals.

The differential input voltage (V_P–V_N) is transferred to current at the Z port by a first transconductance gain (g_{mF}) and the corresponding voltage drop at the Z port is transferred to current at the X port by a second transconductance gain (g_{mS}). Both transconductances can be controlled electronically by external bias currents. The recognized port relations of an ideal VDTAs can be expressed by the following matrix notation (Paul & Pal., 2021):

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ I_X \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 & 0 \\ 0 & 0 & 0 & g_{mS} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ V_Z \end{bmatrix} \quad (1)$$

The two electronically tunable transconductances g_{mF} and g_{mS} of VDTAs can be expressed as:

$$g_{mF} = \frac{(g_{m1} + g_{m5})}{2} \text{ or } g_{mF} = \frac{(g_{m2} + g_{m6})}{2} \quad (2)$$

$$g_{mS} = \frac{(g_{m3} + g_{m7})}{2} \text{ or } g_{mS} = \frac{(g_{m4} + g_{m8})}{2} \quad (3)$$

where $g_{mi} = \sqrt{I_{Bi} C_{ox} \mu_i (\frac{w}{L})_i}$ is the value of transconductance, I_{Bi} is the bias current of ith transistor, C_{ox} is the gate-oxide capacitance per unit area, μ_i is the carrier mobility for PMOS or NMOS transistors, w is the effective channel width and L is the length of the ith transistor (i = 1, 2,…, 8), respectively.

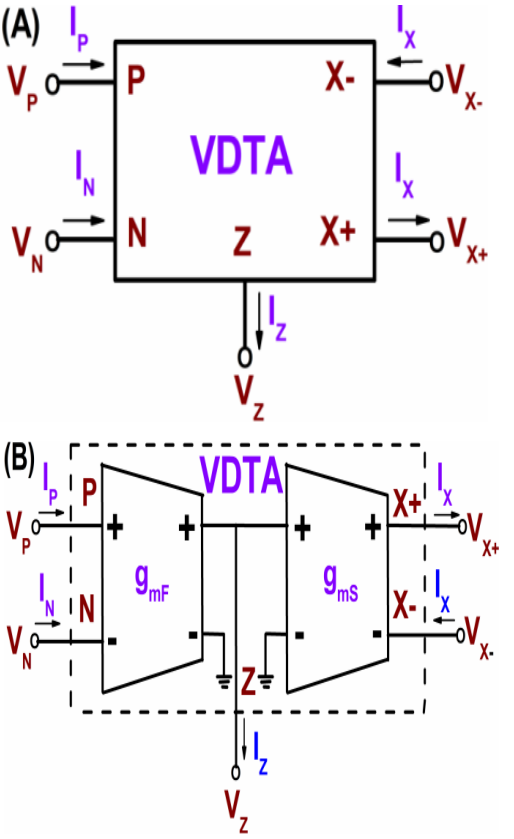
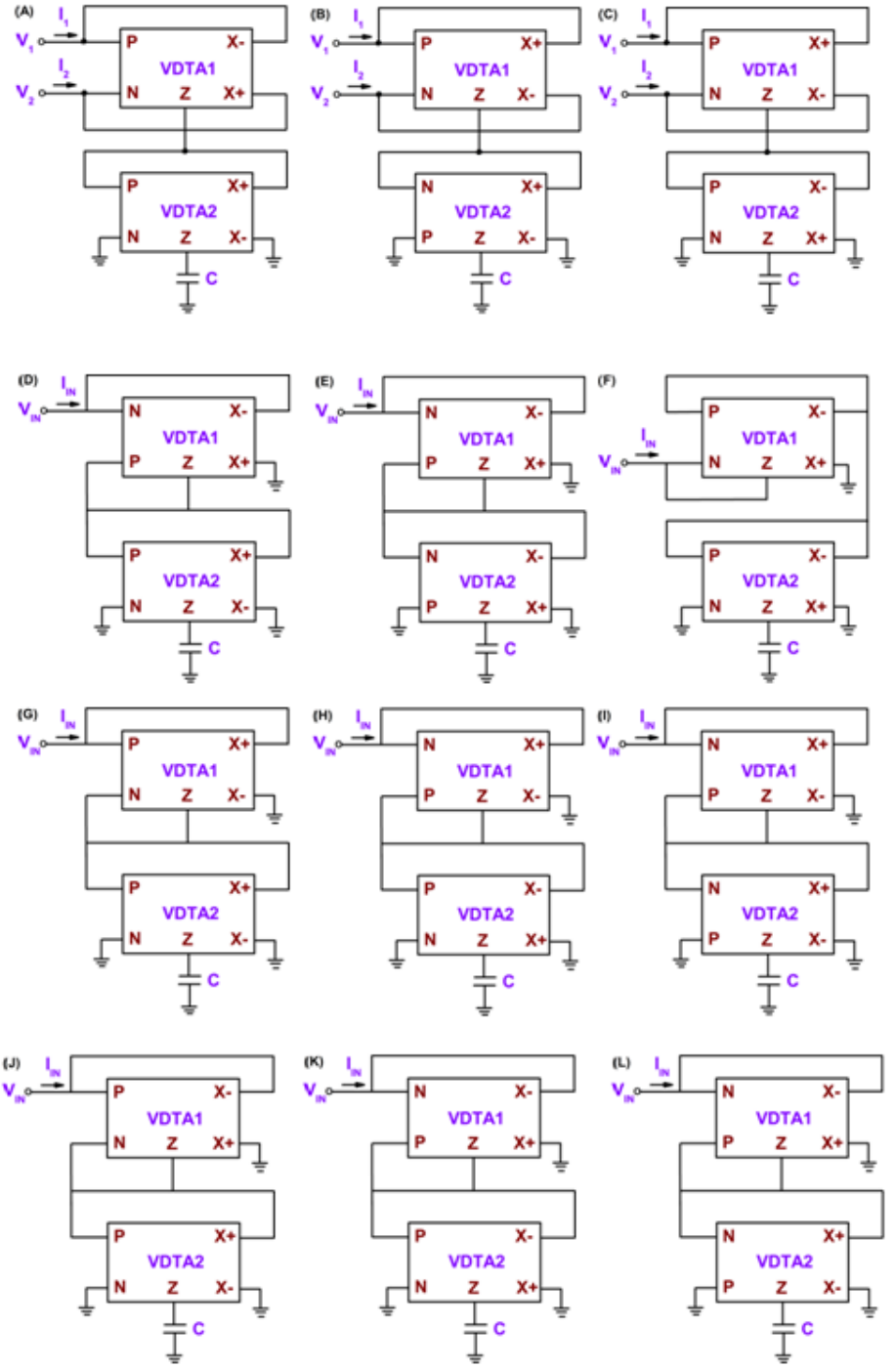
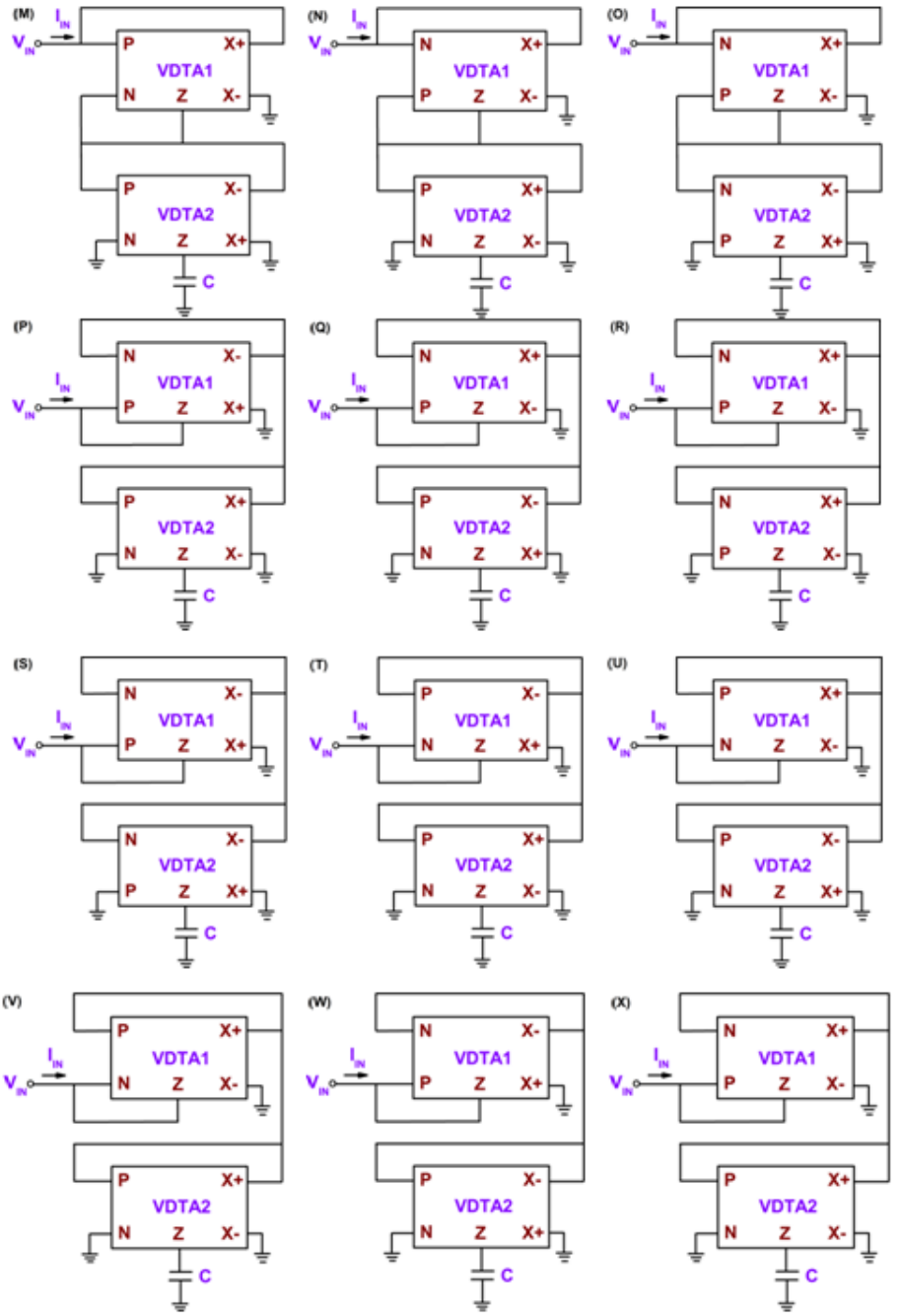


Figure 1. VDTAs (Paul & Pal., 2021): (A) Symbolic representation (B) Inner block diagram

3. Proposed Capacitance Multiplier Circuits

Figure 2 indicates the catalog of the proposed configurations to realize lossy and lossless CM. All the proposed configurations consist of two VDTAs and one grounded capacitor. Using Equation (1) and doing routine analysis, the input impedances of the proposed circuits have been tabulated in Table 1.


(A)
(B)
(C)
(D)
(E)
(F)
(G)
(H)
(I)
(J)
(K)
(L)
VDTA1
VDTA2
C


(M)
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VDTA1
VDTA2
C

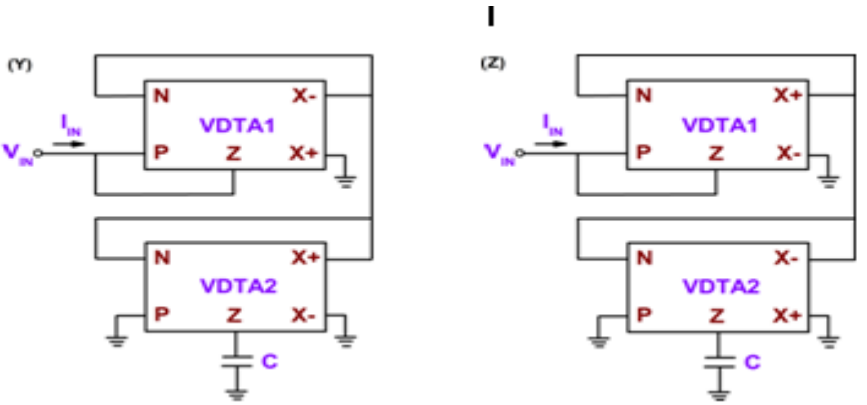

Figure 2. Catalog of the proposed VDTAs-based capacitance multiplier

Table 1. The actively realizable constructions.

Circuit	Simulator type	Impedance realized	Ceq	Req
Figures 2(A)–2(C)	Negative capacitance multiplier	$-\frac{g_{mF2}g_{mS2}}{sCg_{mF1}g_{mS1}}$	$-\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	--
Figures 2(D) – 2(E)	Resistance in series with CM	$\frac{g_{mF2}g_{mS2}}{sCg_{mF1}g_{mS1}}+\frac{1}{g_{mS1}}$	$\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$\frac{1}{g_{mS1}}$
Figure 2(F)	Resistance in parallel with CM	$\frac{1}{\frac{sCg_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}+g_{mF1}}$	$\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$\frac{1}{g_{mF1}}$
Figures 2(G) – 2(I)	Negative resistance in series with CM	$\frac{g_{mF2}g_{mS2}}{sCg_{mF1}g_{mS1}}-\frac{1}{g_{mS1}}$	$\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$-\frac{1}{g_{mS1}}$
Figures 2(J)–2(L)	Resistance in series with negative CM	$-\frac{g_{mF2}g_{mS2}}{sCg_{mF1}g_{mS1}}+\frac{1}{g_{mS1}}$	$-\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$\frac{1}{g_{mS1}}$

Figures 2(M)-2(O)	Negative resistance in series with negative CM	$-\frac{g_{mF2}g_{mS2}}{sCg_{mF1}g_{mS1}}-\frac{1}{g_{mS1}}$	$-\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$-\frac{1}{g_{mS1}}$
Figures 2(P) – 2(S)	Negative resistance in parallel with CM	$\frac{1}{\frac{sCg_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}-g_{mF1}}$	$\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$-\frac{1}{g_{mF1}}$
Figures 2(T) – 2(U)	Resistance in parallel with negative CM	$\frac{1}{-\frac{sCg_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}+g_{mF1}}$	$-\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$\frac{1}{g_{mF1}}$
Figures 2(V) – 2(Z)	Negative resistance in parallel with negative CM	$\frac{1}{-\frac{sCg_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}-g_{mF1}}$	$-\frac{g_{mF1}g_{mS1}C}{g_{mF2}g_{mS2}}$	$-\frac{1}{g_{mF1}}$

Table 1 illustrates that the equivalent resistance and capacitor values can be tuned electronically by changing the bias currents of VDTAs. Also, the circuits do not require any component matching conditions. Here,

$$C_{eq}=\pm\frac{g_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}C=\pm K_iC \qquad (4)$$

where, K_i represents the multiplication factor of ith CM in Figure 2 (i = 1, 2, …, 26). According to Table 1, it is evident that the proposed circuits can realize lossy and lossless capacitance multiplier with

$$C_{eq}=\pm\frac{g_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}C \qquad (5)$$

The multiplication factor (K) depends on the value of g_{mF1}, g_{mS1}, g_{mF2} and g_{mS2} and equal to $\frac{g_{mF1}g_{mS1}}{g_{mF2}g_{mS2}}$. The sensitivity coefficients of the K

with respect to, g_{mF1}, g_{mS1}, g_{mF2} and g_{mS2} are calculated and expressed in Equation (6).

$$S_{g_{mF1}}^{K} = S_{g_{mS1}}^{K} = -S_{g_{mF2}}^{K} = -S_{g_{mS2}}^{K} = 1 \quad (6)$$

According to Equation (6), it is confirmed that the sensitivity is no more than unity. Thus, the sensitivity is under considerable limits.

4. Non-ideal Analysis

In the non-ideal environment of VDTAs, its terminal characteristic can be rewritten as:

$$I_Z = \beta_{Fi} g_{mFi} \left(V_P - V_N \right) \quad (7)$$

$$I_X = \beta_{Si} g_{mSi} V_Z \quad (8)$$

β_{Fi} and β_{Si} are the tracking errors of ith VDTAs.

To verify the performance of the reported circuits under non ideal case, all the circuits are reanalyzed using equations (7)-(8). The newly modified input admittances, equivalent capacitances & equivalent resistors of proposed circuits can be expressed in Table 2.

Table 2. Input impedance, equivalent capacitor and equivalent resistor under non-ideal circumstances.

Circuit	Impedance Realized	C_{eq}	R_{eq}
Figures 2(A)–2(C)	$-\frac{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}}{sC\beta_{F1}\beta_{S1} g_{mF1} g_{mS1}}$	$-\frac{\beta_{F1}\beta_{S1} g_{mF1} g_{mS1} C}{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}}$	--
Figures 2(D)–2(E)	$\frac{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}}{sC\beta_{F1}\beta_{S1} g_{mF1} g_{mS1}} + \frac{1}{\beta_{S1} g_{mS1}}$	$\frac{\beta_{F1}\beta_{S1} g_{mF1} g_{mS1} C}{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}}$	$\frac{1}{\beta_{S1} g_{mS1}}$
Figures 2(F)	$\frac{1}{\frac{sC\beta_{F1}\beta_{S1} g_{mF1} g_{mS1}}{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}} + \beta_{F1} g_{mF1}}$	$\frac{\beta_{F1}\beta_{S1} g_{mF1} g_{mS1} C}{\beta_{F2}\beta_{S2} g_{mF2} g_{mS2}}$	$\frac{1}{\beta_{F1} g_{mF1}}$

Figures 2(G)–2(I)	$\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} - \frac{1}{\beta_{S1}g_{mS1}}$	$\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$-\frac{1}{\beta_{S1}g_{mS1}}$
Figures 2(J)–2(L)	$-\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} + \frac{1}{\beta_{S1}g_{mS1}}$	$-\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$\frac{1}{\beta_{S1}g_{mS1}}$
Figures 2(M)–2(O)	$-\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} - \frac{1}{\beta_{S1}g_{mS1}}$	$-\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$-\frac{1}{\beta_{S1}g_{mS1}}$
Figures 2(P)–2(S)	$\frac{1}{\frac{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}} - \beta_{F1}g_{mF1}}$	$\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$-\frac{1}{\beta_{F1}g_{mF1}}$
Figures 2(T)–2(U)	$\frac{1}{-\frac{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}} + \beta_{F1}g_{mF1}}$	$-\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$\frac{1}{\beta_{F1}g_{mF1}}$
Figures 2(V)–2(Z)	$\frac{1}{-\frac{sC\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}} - \beta_{F1}g_{mF1}}$	$-\frac{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}C}{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}$	$-\frac{1}{\beta_{F1}g_{mF1}}$

It can be seen from Table 2 that even under non-ideal case, the behaviour of proposed circuits remains unhampered although values are slightly deviated from its ideal value. However, for matched VDTAs, $\beta_{F1} = \beta_{F2}$ and $\beta_{S1} = \beta_{S2}$, the value of the equivalent capacitors does not change.

5. Parasitic Analysis

The parasitic effects of VDTAs on the performance of NCM circuit are discussed. The parasitic model of VDTAs is portrayed in Figure 3. For an ideal ith VDTAs, the parasitic resistances R_{Pi}, R_{Ni}, R_{Zi}, and R_{Xi} appearing in parallel at the corresponding terminals P, N, Z and X are approximately equal to infinity, and the parasitic capacitances

C_{Pi}, C_{Ni}, C_{Zi}, and C_{Xi} are approximately equal to zero. Considering these parasitic impedances, the input currents are expressed in Equations (9) and (10). In order to consolidate the currents, some assumptions have been made, as represented in the Equation (11).

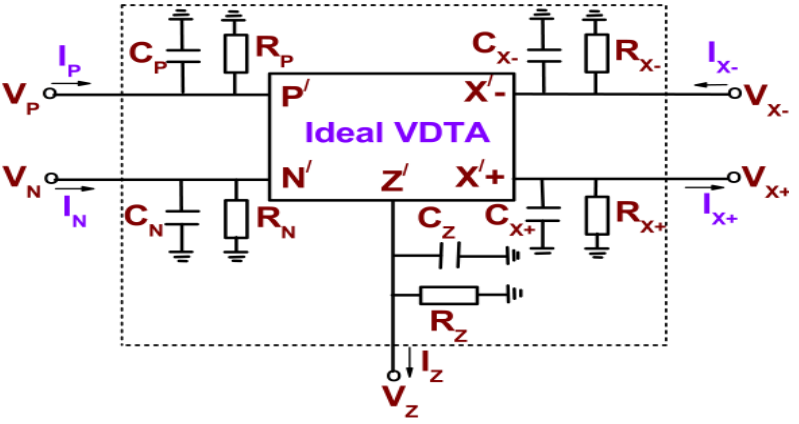

Figure 3. Non-ideal VDTAs showing its parasitic impedances

$$I_1 = \frac{g_{mF1}g_{mS1}(V_1 - V_2)}{-\frac{g_{mF2}g_{mS2}}{sC_{E4} + \frac{1}{R_{Z2}}} + \left(sC_{E3} + \frac{1}{R_{E3}}\right)} + V_1\left(sC_{E1} + \frac{1}{R_{E1}}\right) \tag{9}$$

$$I_2 = \frac{g_{mF1}g_{mS1}(V_2 - V_1)}{-\frac{g_{mF2}g_{mS2}}{sC_{E4} + \frac{1}{R_{Z2}}} + \left(sC_{E3} + \frac{1}{R_{E3}}\right)} + V_2\left(sC_{E2} + \frac{1}{R_{E2}}\right) \tag{10}$$

$$\left.\begin{aligned} C_{E1} &= C_{P1} + C_{X1-} \\ C_{E2} &= C_{N1} + C_{X1+} \\ C_{E3} &= C_{P2} + C_{X2+} + C_{Z1} \\ C_{E4} &= C + C_{Z2} \\ R_{E1} &= R_{P1} \,||\, R_{X1-} \\ R_{E2} &= R_{N1} \,||\, R_{X1+} \\ R_{E3} &= R_{P2} \,||\, R_{X2+} \,||\, R_{Z1} \end{aligned}\right\} \tag{11}$$

Though the input currents are affected due to the inclusion of VDTAs parasitic, it is not obsessive as R_{P1}, R_{N1}, R_{Z1}, R_{X1+}, R_{X1-}, R_{P2}, R_{Z2} and R_{X2+} are very high and C_{P1}, C_{N1}, C_{Z1}, C_{X1+}, C_{X1-}, C_{P2}, C_{X2+} and C_{Z2} are very low. It may be concluded from the Equations (9) and (10) that the proposed NCM work well under the influence of the device parasitics. The input impedances for all the CMs can also be deduced in a similar manner.

6. Application Examples

In this section, two analog application examples are provided to confirm the usability of the proposed NCM. The first application example is the capacitive cancellation scheme in which the parasitic capacitors present in the output circuits are cancelled. Figure 4 depicts the capacitive cancellation circuit schematic. In this circuit, the negative capacitor has been constructed with the proposed negative lossless grounded CM in Figure 2(A).

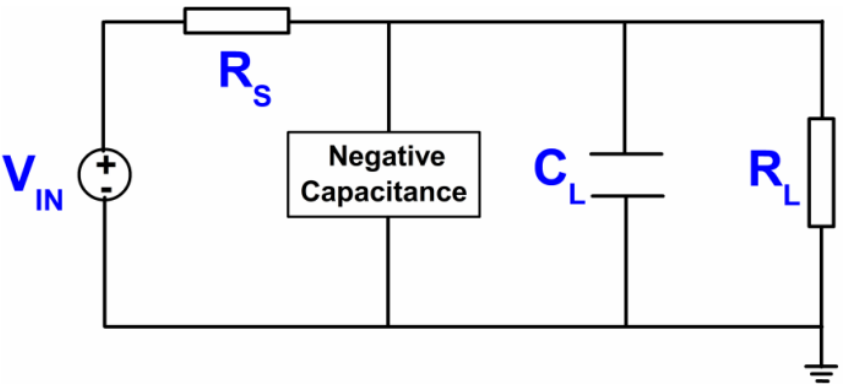

Figure 4. The capacitance cancellation circuit

The second application example is a voltage mode sinusoidal oscillator. We have constructed the oscillator circuit by modifying the oscillator circuit proposed in (Banerjee et al., 2019) to use the negative capacitance in place of the positive capacitor. The circuit schematic of the oscillator is depicted in Figure 5. The circuit uses a single VDTAs and two capacitors. The capacitor C_1 is implemented using the proposed negative lossless CM in Figure 5. The routine

circuit analysis of the oscillator circuit yields the characteristic equation and oscillation frequency as follows.

$$s^2 C_1 C_2 + g_{mF} g_{mS} = 0 \tag{12}$$

$$\omega_o = 2\Pi f_O = \sqrt{\frac{g_{mF} g_{mS}}{C_1 C_2}} \tag{13}$$

The two quadrature voltages (V_{O1} and V_{O2}) are related as:

$$\frac{V_{O2}}{V_{O1}} = -\frac{sC_1}{g_{mS}} \tag{14}$$

Equation (14) confirms that the output voltages are in quadrature signals.

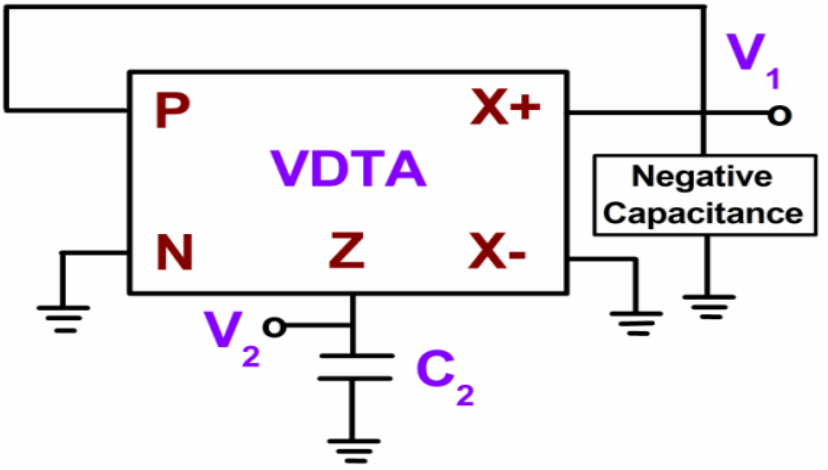

Figure 5. Quadrature oscillator employing a grounded negative capacitance

7. Results & Discussion

To verify the theoretical predictions and application of the proposed capacitance simulator, the PSPICE simulation has been employed. Figure 6 displays schematic descriptions of the VDTAs used in the simulations. The VDTAs was implemented using TSMC 0.18 µm CMOS process parameters with ± 0.9 V power supply. The aspect ratios of the MOS transistors were chosen as: 3.6/0.36 and 16.64/0.36 for M1-M4 and M5-M8, respectively. The capacitance simulator in Figure 2(A) is selected as an illustration to examine the performance.

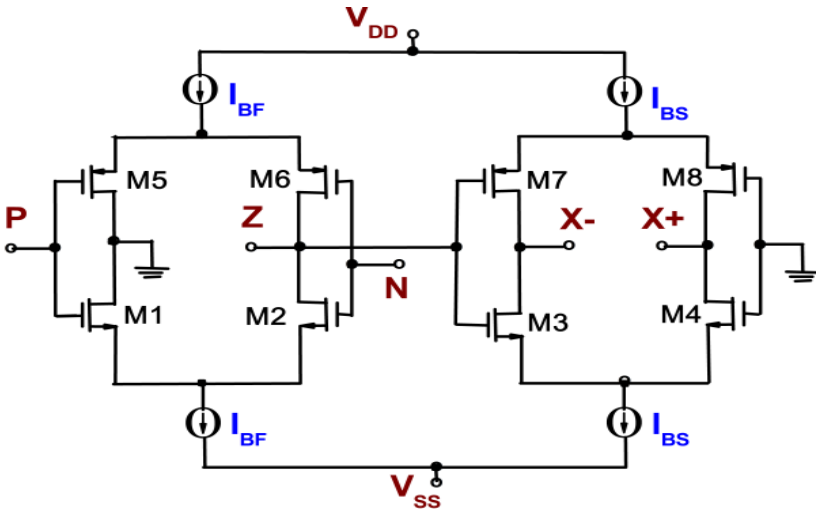

Figure 6. CMOS based internal circuit construction of VDTAs

The workability of the proposed NCM is contemplated using the following simulations conditions:

- C is constant while K changes;
- K is constant while C changes; and
- K and C have fixed and varying temperatures.

Detailed simulation arrangements are given in Table 3. Simulated and ideal frequency responses of the input impedance of Figure

2(A) for various multiplication factors are shown in Figure 7. To achieve the multiplication factor to the values of K = 5, K = 10, and K = 25, the bias current I_{B1} (I_{BF1} = I_{BS1} = I_{B1}) is kept constant at 150 µA, whereas the bias current I_{B2} (I_{BF2} = I_{BS2} = I_{B2}) is set to 36 µA, 22 µA, and 13 µA, which results in: C_{eq} = 5 nF, 10 nF, and 25 nF, respectively. For various capacitance values with fixed K, the simulated and ideal frequency responses are illustrated in Figure 8. It is seen that the simulation results appear to be in good agreement according to the frequency response of the simulated and ideal capacitors given in Figure 7 and 8. The effective value of capacitance and frequency range is also recorded in Table 3. In order to confirm the temperature-insensitivity of the multiplication factor of the proposed circuit of Figure 2(A), simulations are performed at t = – 40 °C, 27°C and 110°C for K = 10 and C = 100 nF and the graphical representation is shown in Figure 9. The results in Figure 9 are satisfying because the curves of impedance of proposed capacitance simulator are slightly affected by temperature.

The time-domain analysis of proposed multiplier is also performed by selecting the following component values: I_{B1} = 150 µA, I_{B2} = 36 µA, and C = 1 nF and applying a sinusoidal signal with 1 MHz frequency and an amplitude of 30 µA. The obtained waveforms are attached in Figure 10, which confirms that current leads the voltage.

Table 3. Detailed simulation settings and summary of observations.

Case	Components tuning			Realized C (nF)	Magnitude response within 10% error
	C (nF)	K	Temperature (°C)		
1	1	5	27	5	5.495 kHz to 4.37 MHz
		10		10	6.166kHz to 2.69 MHz
		25		25	3.235 kHz to 851.138 kHz
2	0.5	10	27	5	123.027 kHz to 5.25 MHz
	2			20	3.092 kHz to 1.35 MHz
	5			50	1.231 kHz to 549.541 kHz
3	100	10	– 40	1000	11 Hz to 3.548 kHz
			27	1000	Up to 2.754 kHz
			110	1000	Up to 2.371 kHz

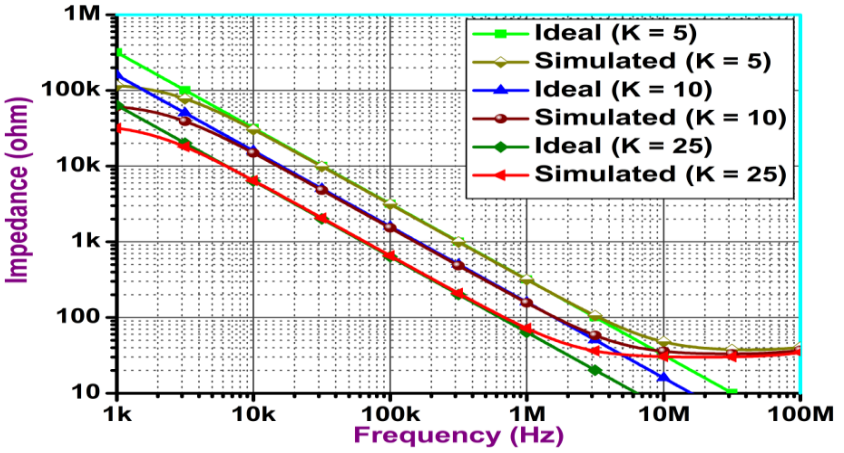

Figure 7. Magnitude responses of the input impedance of the proposed capacitance multiplier and ideal capacitor for K = 5, 10 and 25 selecting C = 1 nF

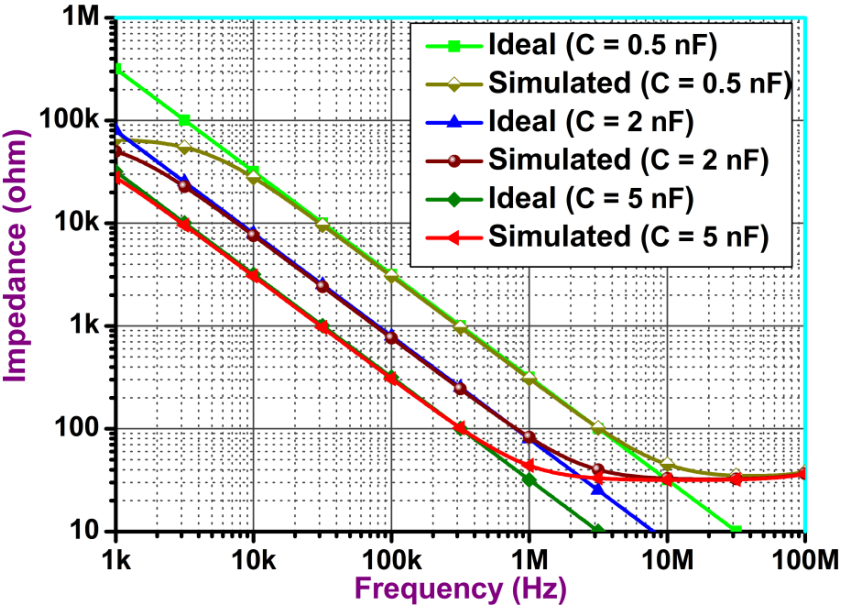

Figure 8. Magnitude responses of the input impedance of the proposed capacitance multiplier and ideal capacitor for C = 0.5, 2 and 5 nF by selecting K = 10

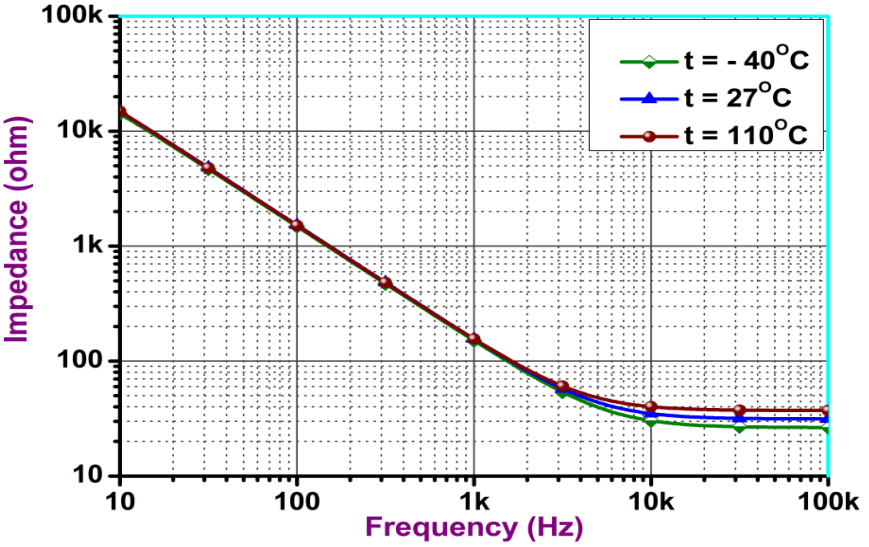

Figure 9. Magnitude responses of the input impedance of the proposed capacitance multiplier and ideal capacitor for t = – 40°C, 27°C and 110°C by selecting C = 100 nF and K = 10

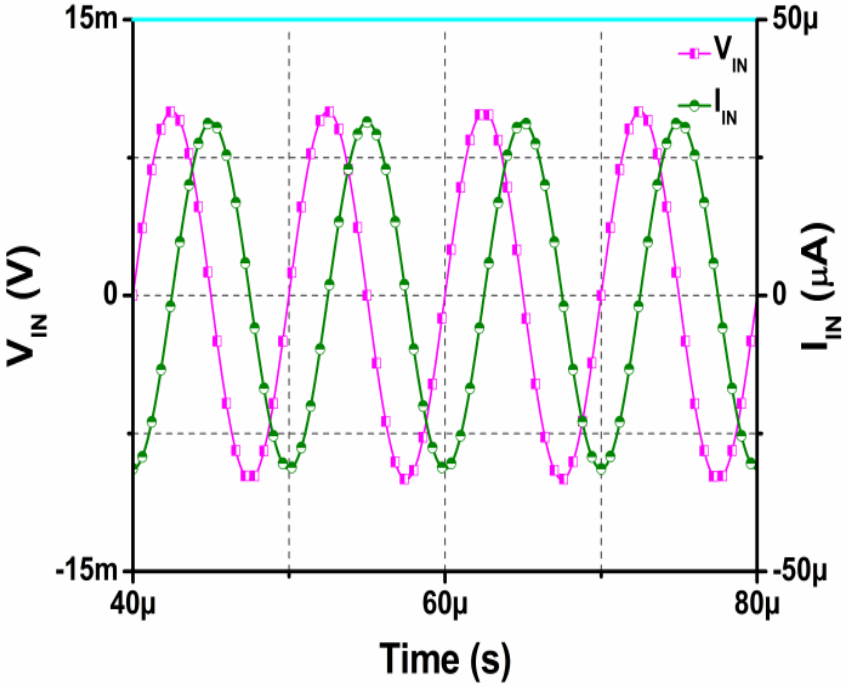

Figure 10. Transient response of the proposed capacitance multiplier

Monte Carlo analysis is also done for 100 times to show the variation in equivalent capacitance value depending upon capacitor tolerances. Multiplication factor is chosen as five (I_{B1} = 150 µA, I_{B2} = 36 µA, and C = 1 nF). Assuming capacitor tolerances of 5%, response is recorded and portrayed in Figure 11 in the form of a histogram. Detailed statistical parameters are also included in Figure 11. It illustrates that the magnitude of equivalent capacitances varies from 4.60642 nF to 5.03548 nF with a mean value of 4.82936 nF, which indicates that the mismatch in the capacitor values does not have a large effect on the equivalent capacitance value.

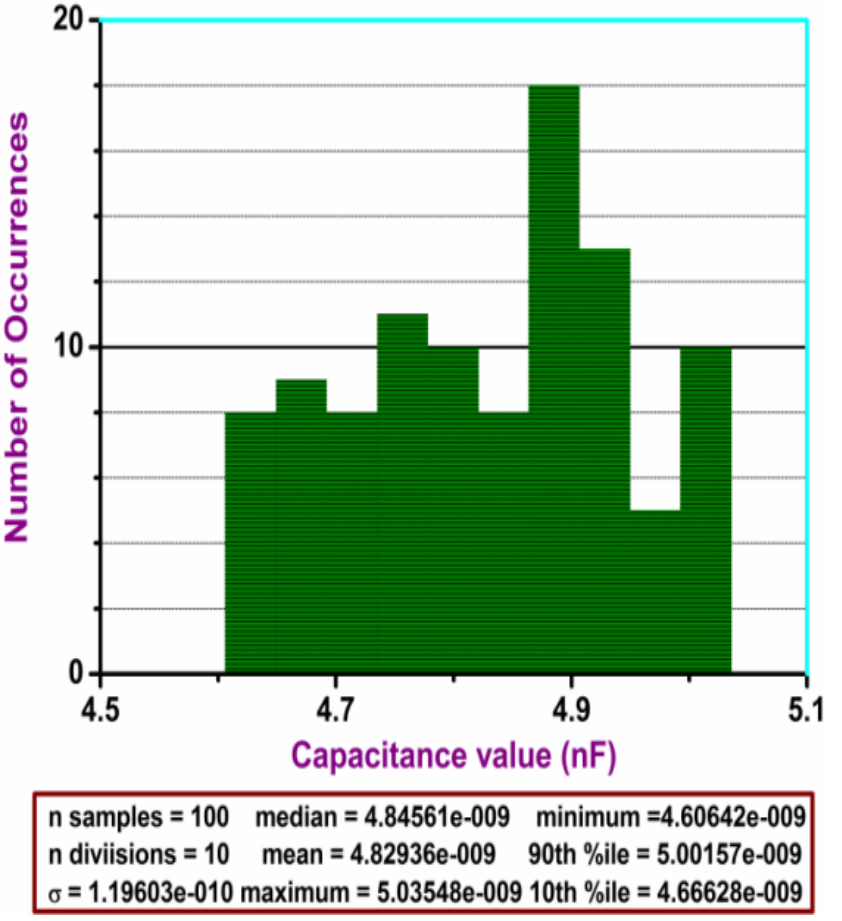

Figure 11. Monte Carlo analysis for capacitance multiplier circuit

The negative capacitance multiplier finds a crucial application in designing capacitance cancellation circuits. The capacitance cancellation circuit is portrayed in Figure 4. The component values chosen for the circuit are C_L = 0.5 nF and R_S = R_L = 1 kΩ. A sine wave with 800 mVp-p of 100 kHz frequency is applied as an input. The current outputs through resistors R_S and R_L are depicted in Figure 12. It is notable that the capacitance (C_L) in the design has been eliminated by the NCM.

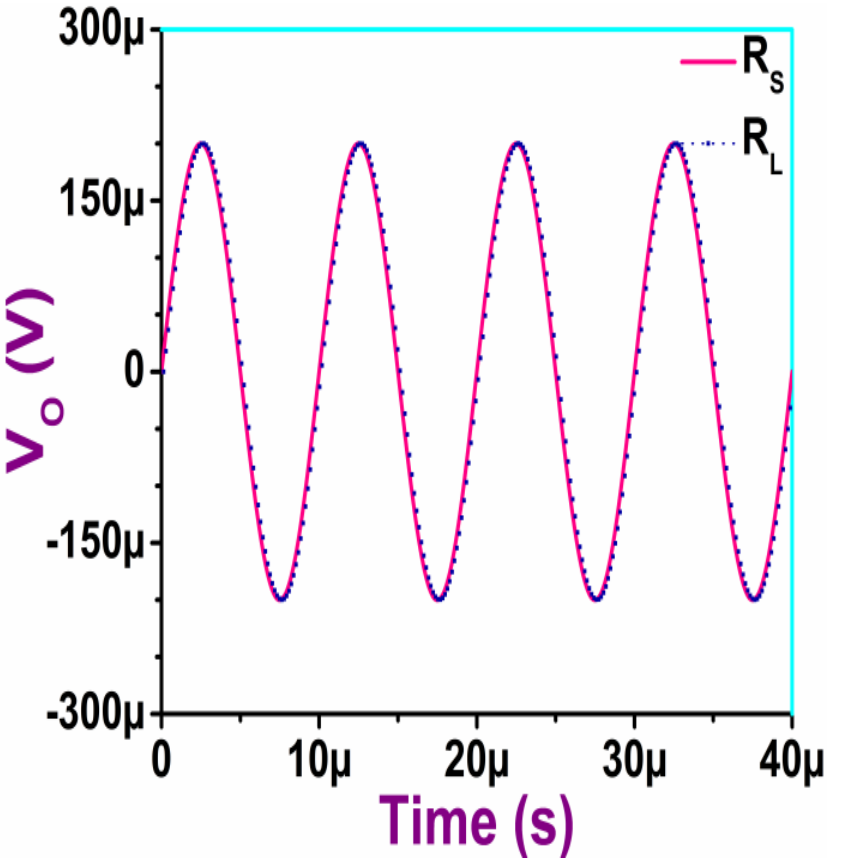

Figure 12. The typical waveforms of the current through *Rs* and R_L

For better confirmation of the performance of the CM, the proposed negative capacitance multiplier circuit is utilised in the configuration of the quadrature sinusoidal oscillator illustrated in Figure 5. The component values are selected as C_1 = 0.5 nF, I_{BF1} =

I_{BF2} = I_{BS1} = I_{BS2} = 150 µA for the oscillator circuit. For the grounded negative capacitance simulator, the components values are selected as C_1 = 0.05 nF, I_{B1} = 150 µA and I_{B2} = 22 µA. The steady-state responses of the oscillator circuit are illustrated in Figure 13. The simulated oscillation frequency of 223.95 kHz concur with the theoretical value of 224.09 kHz. Theoretically, the angle difference between the two outputs, i.e., V_{02} and V_{01}, must be 90^0. However, the calculated angle difference between the two voltage signals is derived as 88.70.

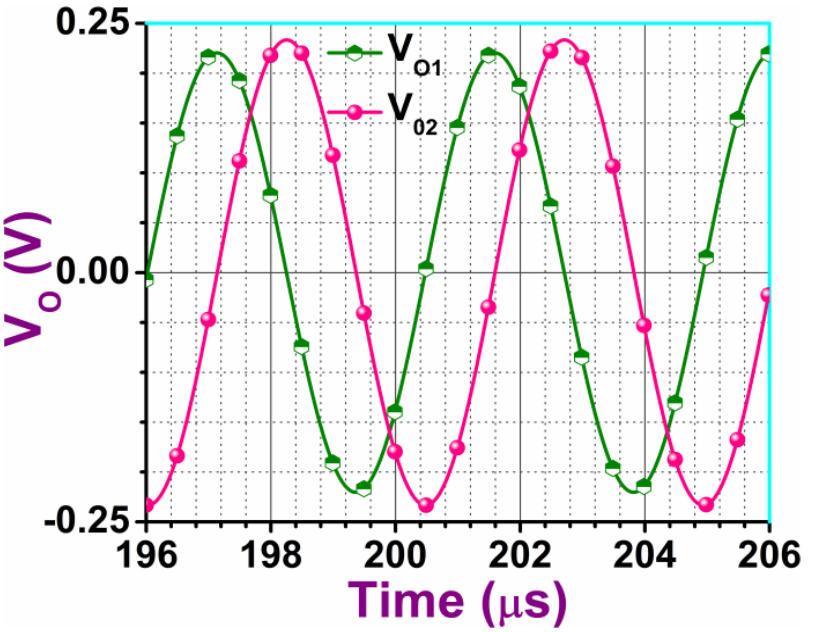

Figure 13. Steady-state waveform of the voltage outputs

8. Comparison with previous publication

The proposed VDTAs based CMs are compared with the previously published works on the basis of resistorless structure; possibility of tuning electronically; type of capacitor used; active and passive components required. The findings are summarized in Table 4. It may be seen that

- Resistance was required in the structures for the circuits referred in (Özer, 2021; Stornelli et al., 2021; Biolek et al., 2019; Gupta et al., 2019; Nagar & Paul, 2021; Dogan & Yuce, 2020; Özer et al., 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020; Al-Absi & Abulema'atti, 2019; Yesil et al., 2017) but in our work, this is eliminated.
- The equivalent capacitance value was not electronically tunable in references (Stornelli et al., 2021; Biolek et al., 2019; Nagar & Paul, 2021; Dogan & Yuce, 2020; Özer et al., 2020; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020; Yesil et al., 2017), whereas the proposed topologies offer electronic tuning facilities.
- A relatively large supply voltage was required in the structures for the circuits referred in (Siripruchyanun et al., 2019; Singh et al., 2020; Jaikla & Siripruchyanan, 2006; Kamath, 2018; Kamat et al., 2011) than the proposed ones.
- The capacitance multiplier circuits mentioned in references (Özer, 2021; Stornelli et al., 2021; Biolek et al., 2019; Tangsrirat et al., 2019; Nagar & Paul, 2021; Abuelma'atti, 2012; Lahiri & Gupta, 2011; Abuelma'atti & Dhar, 2016; Abuelma'atti et al., 2017; Channumsin & Tangsrirat, 2016; Singh et al., 2020; Rivera-Escobar et al., 2013; Al-Absi et al., 2019) used floating capacitor/s, while the proposed CMs use grounded capacitors.

The proposed CMs and the CMs of Ref (Tangsrirat & Unhavanich, 2016) are electronically tunable and use only two active blocks, one capacitor. The circuit of ref (Tangsrirat & Unhavanich, 2016) realizes only one positive capacitance multiplier whereas the proposed circuits realize negative capacitance multipliers and lossy capacitance multipliers. Table 4 confirms that the proposed configurations provide better advantages in all aspects.

Table 4. Comparison of the proposed work with the previously developed one.

Ref.	Building Block	Type	Supply Voltage (V)	Power Consumption	Technology	No of passive elements	Tunable?
Özer, 2021	2 CFTA	Positive lossless (Figures 4 & 5)	± 0.75	Not reported	0.13 µm	2 R (G) + 1 C (F)	Yes
		Negative lossless (Figures 6 & 7)					
Stornelli, et al., 2021	1 VCII+ & 1 VCII– (Figure 3)	Positive lossless	± 1.65	1.5 mW	0.35 µm	2 R(1 F, 1 G) +1C (F)	No
	2 VCII+ (Figure 4)	Negative lossless					
Biolek et al., 2019	1 CDTA (Figure 3)	Positive lossless	± 5	Not reported	0.7 µm	1 R (G) + 1 C (F) (Figures 3a, 4a)	Yes
	1 CDTA+1 DVA (Figure 4)					2 R(1 G, 1 F) +1C (F) (Figures 3b, 4b)	No
Gupta et al., 2019	2 VDCC	Positive lossless	± 0.9	Not reported	0.18 µm	2 R (G) + 1 C (G)	Yes
Siripruchyanun et al., 2019	1 CCCCTA, 1 COA	Positive lossless	± 2.5	13.4 mW	0.5 µm	0	Yes
Tangsrirat et al.,	1 VDGA	Positive lossless	± 1	1.09 mW	0.25 µm	0 + 1 (F)	Yes

2019							
Singh et al., 2020	1 CCIIITA	Positive lossless	± 1.5	0.974 mW	0.18 µm	0 + 1 (G)	Yes
Nagar & Paul, 2021	2 OTRA, 1 VF (Figures 3(C), (D))	Positive lossless	± 0.9	0.833 mW	0.18 µm	2 R (F) + 1 C (F)	No
Dogan & Yuce, 2020	2 CFOA	Positive lossless	± 9	233 mW	AD844	2 R (F) + 1 C (G)	No
Özer et al., 2020	2 CFOA (Figure 3)	Positive lossless (Circuit A)	± 0.75	Not reported	0.13 µm	2 R(1 G, 1 F)+ 1 C(G)	No
		Series RC (Circuit B)				3 R(1 G, 2 F) + 1C (G)	
		–R Series with C (Circuit C)				2 R(1 G,1 F) + 1C(G)	
		R parallel with C (Circuit D)				3 R(2 G, 1 F) + 1C(G)	
		R parallel with C (Circuit E)				3 R(2 G, 1 F) + 1C(G)	
Lahiri & Gupta, 2011	2 CFOA (Figures 2 A1-A2, Figures 3 B1-B2)	Negative lossless	± 2.5	Not reported	0.35 µm	2 R (G) + 1C (G)	No
	1 CFOA (Figure 4)					2 R (1G, 1F + 1 C (F)	

	1 CFOA (Figure 5)					2 R (F) + 1C (G)	
Abuelma'atti & Dhar, 2016	3 CFOA	Negative frequency dependent resistor with series C (Figures 1(A), 1(B))	± 5	Not reported	AD844	2 R (F) + 1 C (F)	No
		Positive lossless (Figure 1(C)) Negative lossless (Figure 1(D))					
Abuelma'atti et al., 2017	2 CFOA	– R Series with – C (Figure 1(C). Figure 1(G), case I)	Not reported	Not reported	Not reported	2 R (F) + 1 C (F)	No
		Series – R– C (Figure 1(C). Figure 1(G))				1 R (F) + 2 C (F)	
		Series – R, + conductance with – C (Figure 1(D). Figure 1(G))				1/2 R (F) + 2 C (F)	
		– R Series with – C				2 R (F) + 1 L (F)	

		(Case III Figure 1(C), Figure1(G))					
		+ C divider (Case IV Figures 1(A), 1(E))				2/4R(1/2 G,1/2F)+ 1C(F)	
		-C divider (Figure 1(B),1(C),1(G))				2/3 R (F) + 1 C (F)	
		Lossless C (Figure (F))				4 R(2 G, 2 F) +1C (F)	
		–C series with –R (Figure 1(D))				3 R (F) + 1 C (F)	
		Series – C – R (Figure 1(D), case IV, V)				2/3 R (F) + 1/2 C (F)	
Channumsin & Tangsrirat, 2016	2 CFOA	Positive lossless (Figure 2)	± 0.75	Not reported	0.35 µm	2 R (1 G, 1 F) +1 C (F)	No
Abuelma'atti, 2012	1 CFOA	Series –CR (Figure 2, realization B)	± 15	Not reported	AD844	3 R (1 G, 2 F) +1 C (F)	No
		Negative lossless (Figure 3, case C)				2 R (1 G, 1 F) +1 C (G)	

Singh et al., 2020	2 CFOA (Figure 2)	Negative lossless	± 5 (AD844A) ± 1.8 (OTA)	Not reported	AD844	2 R (F) + 1 C (F)	No
	2 CFOA + 2 OTA (Figure 3(A))	Positive lossless				0 + 1 C (F)	Yes
	2 CFOA+2 OTA (Figure 3(B))	Negative lossless				0 + 1 C (F)	Yes
Jaikla & Siripruchyanan, 2006	4 OTA	Positive lossless	± 2.5	0.565 mW	PR200N & NR200N	0 + 1 C (G)	Yes
Rivera-Escobar et al., 2013	3 OTA (Figure 2)	Positive lossless	± 2	6.72 mW	0.5 µm	0 + 1 C (F)	Yes
Kamath, 2018	1 DO-OTA (Figure 3(A))	Lossy	Not reported	Not reported	Not reported	0 + 1 (G)	Yes
	2 DO-OTA (Figure 3(B))	Lossless					
Kamat et al., 2011	3 OTA (Figure 2(C))	Negative lossless	± 2	Not reported	0.5 µm	0 + 1 (G)	Yes
	3 OTA (Figure 2(D))					0 + 1 (F)	
	2 OTA (Figure					0 + 1 (G)	

	2(F))						
Al-Absi et al., 2019	1 CCII+, 4 OTA	Positive lossless	± 0.75	2.301 µw	0.18 µm	0 + 1 C (F)	Yes
Al-Absi & Abulema'atti, 2019	1 CCII ±, 1 OTA	Positive lossless	Not reported	Not reported	LM13700AN, AD844	1 R (G) + 1 C (G)	Yes
		Negative lossless					
Yesil et al., 2017	1 CCII –, 1 VF (Fig. 1)	Positive lossless	± 0.9	Not reported	0.18 µm	2 R (F) + 1 C (G)	No
	1 ICCII, 1 IVF (Fig. 2)						
Tangsrirat & Unhavanich, 2014	2 VDTAs	Positive lossless	± 1.8	Not reported	0.35 µm	0 + 1 C (G)	Yes
This work	2 VDTAs	Negative lossless (Figure 2(A)-2(C))	± 0.9	1.08 mW	0.18 µm	0 + 1 C (G)	Yes
		Lossy (Figure 2(D)-2(Z))					

9. Conclusion

New configurations that can simulate lossy and lossless capacitance multipliers using VDTAs have been proposed. All the proposed circuits use two VDTAs and only grounded capacitors. No component matching constraints are required to realize these configurations. A non-ideal and parasitic analysis is also included. The NCM circuit is studied in detail. The performance of the proposed NCM circuit is tested through the necessary SPICE simulations. Simulation results show that the proposed NCM circuit is feasible for various applications: such as, parasitic cancellation circuit, quadrature sinusoidal oscillator circuit. Therefore, the proposed circuits may provide an effective alternative in the arena of CM design for the researchers.

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