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A Study on Effects of Gate Dielectrics in CNT-FET Using Non-Equilibrium Green's Function Modelling

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Abstract

This study examined how gate dielectric materials affect drain current and quantum capacitance in wrap-around CNTFET devices. We examined CNTFET dielectric materials using Nanohub's FET toy simulator using the NEGF (non-equilibrium Green's function) model. We found that gate-dielectric choice affects the drain current and larger k values produced higher currents despite the same gate and drain voltages. However, the nano-metric device size limits electrons, causing drain current saturation early. Thus, dielectric and operational bias selection must be optimized. For high-k dielectrics, quantum capacitance dropped quickly after peaking. This can be explained by the fact that nano-sized materials have a lower density of energy states.

Key-words: wrap-around CNTFET, FET toy simulator, gate dielectric variation, quantum capacitance.

Introduction

In the past six decades, the process of device scaling has advanced at an exponential rate. This means that the device density on a typical microprocessor chip doubles approximately every two to three years, in accordance with Moore's law. The semiconductor industry will need to continue to scale devices successfully in the years to come in order to sustain its current level of success. This is the culmination

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of assessing and projecting the technical needs of today and tomorrow, and the updates to the 2022 International Roadmap for Devices and Systems are taking into account the work that will be done over the following few years [1]. As a result of this, it has been established that modern CMOS technology has struggled with issues like deteriorated *I-V* characteristics, excessive leakage currents, and poor gate control. Scalability beyond 30 nm is made significantly more difficult and complex by the inherent limitations imposed by the physics of semiconductors [2]. New theories and methods are required for device modelling in order to achieve an understanding of the physics of devices and to design devices at a scale of fewer than 30 nanometres. Nanotechnology is being used to construct nanoscale circuits such as carbon nanotube-based field effect transistor (CNTFET) in order to solve the problems caused by CMOS [3, 4]. They are high-performance ballistic transport devices that use a relatively little amount of power [5]. The high electrical properties of CNTFETs due to the quasi-ballistic effect have sparked interest among the researchers recently, which makes them an appealing option for high-speed applications [6]. This has caused the high electrical properties of CNTFETs to be a topic of discussion among researchers. The temperature of the CNTFET has a significant impact on its characteristics as well as its performance [7]. Scaling CNTFETs has also revealed short channel effects, like elevated leakage currents, sub-threshold instabilities and, drain induced barrier lowering. These effects were observed because of the scaling of the devices. Hence, as the device temperature increases, leakage current deteriorates the performance of the circuit, and makes it difficult to differentiate between the two binary states. It happens due to the fact that silicon dioxide is used in CNTFETs in its dielectric role, which acts as an insulator. Therefore, in place of silicon dioxide, other dielectric materials should be utilized in order to reduce the effects of short channels and the amount of leakage current [8].

Carbon Nanotubes

Iijima developed a needle-like tube-containing finite carbon structure in 1991 by using arc-discharge evaporation [9]. Each needle had a number of coaxial tubes of graphite sheets ranging from two to fifty in total, depending on the size of the needle. These rolled sheets of graphene are carbon nanotubes (CNTs) in their most basic

form. A single walled nanotube is made by rolling a single sheet of graphite, while the combination of two sheets results in a double wall CNT, and the rolling of multiple sheets results in a multi-wall CNT (MWCNT). The rolling of sheets can take one of two forms: a Russian doll model, in which graphite sheets are arranged in concentric circles; or a parachute model, in which a single sheet of graphite is rolled in around itself, resembling a parachute scroll or rolled newspaper [10]. Both of these models are referred to as parachute models to create armchair, zigzag, and chiral carbon nanotubes, graphene sheets are rolled along lattice vectors to create the nanotubes [11]. When attempting to determine the chirality (n, m) of a semiconducting single wall carbon nanotube, it is common practice to make use of a set of empirical equations. If mod (n – m, 3) = 0 a SWCNT (n, m) is metallic, and if mod (n – m, 3) = 1 or 2. Semi-conductivity can be demonstrated in SWCNT (n, m) [12]. This relationship is always found to be true, with the sole exception of extremely small diameter SWCNTs, in which case curvature effects predominate in determining the properties of the material.

Carbon Nanotubes based Field Effect Transistors (CNTFET)

The resilience CMOS devices have to noise and the low static power needs that they have are the two of their most significant advantages. Because CMOS logic devices only consume substantial power from the power source while they are switching between on and off states, they produce significantly less heat than other types of logic devices. This allows CMOS logic devices to have a high density of logic functions. MOS FET technology based on CNTs has been compared to alternative choices, such as sub-10 nanometer Si nanowire transistors and III–IV tunnel FET, by researchers from IBM and Stanford. CNT technology was the only one that was able to deliver significant performance increases when scaled down from an 8 nm technology to a 5 nm technology, while other alternatives did not exhibit any obvious performance advantages [13].

Wrap-around gate CNTFET

Coaxial, wrap-around, or Gate-all-around CNTFETs were initially developed in 2008, and their introduction represents a significant advance in technological capability [14]. Instead of gating only the region of the CNT that is located in close proximity to the gate

contact, the gating affects the full circumference of the nanotube. In an ideal world, this will result in an improvement in the electrical performance of the CNTFET, as well as a reduction in leakage current and an increase in the on/off ratio. Coating carbon nanotubes with a gate dielectric and gate contact via atomic layer deposition is the initial stage in the process of constructing the device [15]. The wrappings are then put on an insulating substrate after a solution is used to deposit a nanotube, which is subsequently partially etched to expose the ends of the nanotube. The contacts for the source, drain, and gate are then placed on the ends of the CNTs and the outside wrapping of the gate, as shown in Fig. 1.

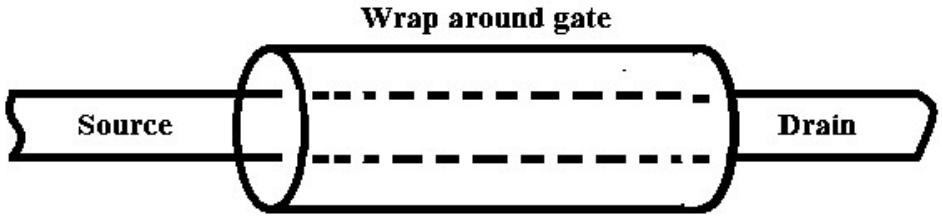

Fig. 1. Schematic for wrap-around gate CNT-FET

Mathematical Modelling

The mathematical model, here used is based on NEGFs (non-equilibrium Green's functions) that treats quantum mechanical transport in nano-devices. The simulation presented in this work, is based on solving the Schrodinger's and Poisson's equations using NEGF. Green's function may be represented as a matrix equation, $G(E) = [EI - H - \varepsilon_S - \varepsilon_D]^{-1}$. Here, E represents energy, I represent the identity matrix, $\boldsymbol{H}$ represents the Hamiltonian of carbon nano-tubes, ε_S and ε_D represents self-energies respectively of source and drain [16]. Using the NEGF formalism, we calculate the concentration of holes (p) and electrons (n) with open boundary conditions and Schrödinger's equation. DoS (density of states) provides the electron concentration as,

$$n = \int_{E_i}^{\infty} [D_S f(E - E_{FS}) + D_D f(E - E_{FD})\, dE$$

where, E_i is the Fermi level of carbon nano-tubes and f(E) is Fermi-Dirac distribution function, D_s is DoS at source, E_{FS} is the Fermi energy at source, etc. After obtaining self-consistency, the currents at the source terminal and drain terminal may be represented by following expression,

$$I = \frac{4q}{h} \int T(E)[f(E - E_{FS}) - f(E - E_{FD})]\, dE$$

where, T(E) is the transmission coefficient calculated by NEGF.

Result and Discussions

In this simulation study, diameter of carbon nanotube is taken as 1 nm, and thickness for gate insulator is taken as 1.5 nm. The dielectric materials for gate insulators are taken as silicon dioxide (3.9), silicon nitride (7), silicon (11.7), paraffin (2.25), zirconia (15), hafnium oxide (25), lanthanum oxide (30) and titania (40) [8, 17]. The various parameters used in this simulation study are elaborated in Fig. 2.

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fettoy input info
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gate insulator thickness      : 1.5e-09 (m)
insulator dielectric constant: 40
temperature                   : 300 (K)
initial gate voltage          : 0 (eV)
final gate voltage            : 1 (eV)
number of bias points (gate)  : 13
initial drain voltage         : 0 (eV)
final drain voltage           : 1 (eV)
number of bias points (drain): 13
threshold voltage             : 0.32
gate control parameter        : 0.88
drain control parameter       : 0.035
Series Resistance             : 0 (ohms)
NT diameter                   : 1e-09 (m)
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Fig. 2. Simulation parameters for wrap-around gate CNT-FET

The variation of drain current with gate voltage for different drain voltages are shown in Fig. 3. It shows that the variation in up-threshold and sub-threshold regions is dependent on the drain voltages. Even a small variation of 0.02V in drain current causes a noticeable dependence, almost a decade, in drain current. This characteristic results in the efficient use of CNT-FET as a switching device as required in modern digital circuitry. The dependence in the sub-threshold region however needs to be optimised.

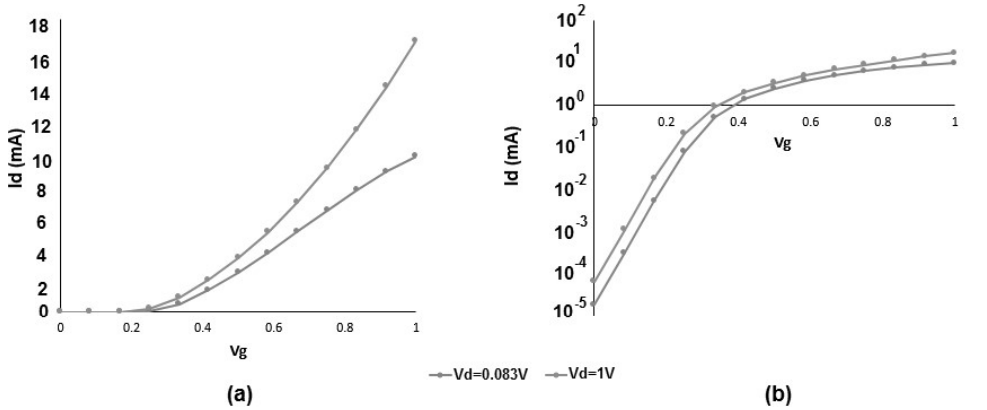

Fig. 3. Variation of drain current with gate voltage for different drain voltages (0.083V & 1V) in (a) linear and (b) logarithmic scales

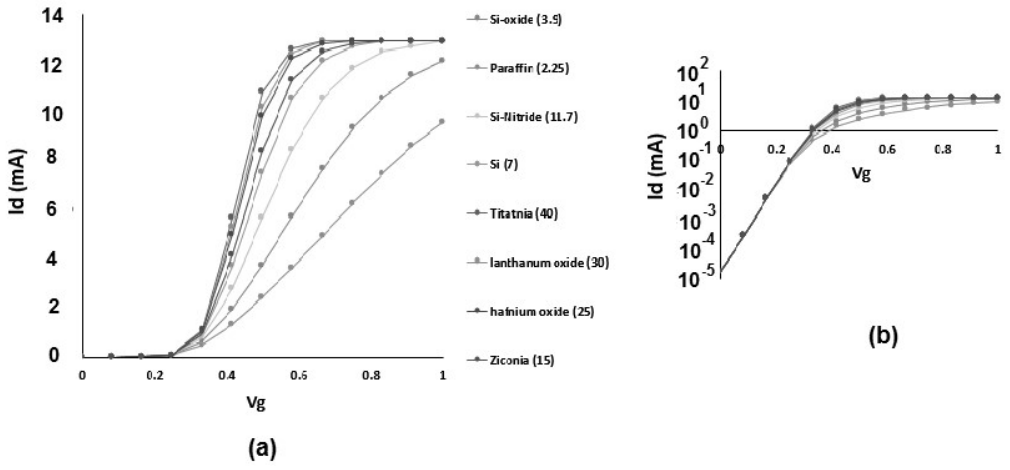

Fig. 4. Variation of drain current with gate voltage for different gate dielectric materials such as paraffin (2.25), silicon dioxide (3.9), silicon nitride (7), silicon (11.7), zirconia (15), hafnium oxide (25), lanthanum oxide (30) and titania (40) in (a) linear and (b) logarithmic scales.

Fig. 4 shows the drain current variation with different gate dielectrics. It is to be noted that at a given gate voltage, the drain current increases as the dielectric constant (k) of the material increases. The drain current, however saturates at lower gate voltages in case of higher gate dielectric constant. In sub-threshold region the drain current is found to be independent of gate-dielectric, however it increases exponentially with gate voltage. In the conduction region, the drain current is found to be varying with dielectrics materials and found to get saturated with a typical value of 10mA. This may be attributed to fixed numbers of electrons in the channel region for nano-scaled devices. The high k dielectric

however, enhances the ability to chop-off these charge carriers early in the gate voltage variation for drain current contribution.
The quantum capacitance variation with different gate dielectrics is shown in Fig. 5. It is observed that typical quantum capacitance increases with the increase in the dielectric constants at a given gate voltage but it starts decreasing at an early gate voltage too. This is attributed to series capacitance that arises due to dielectric insertion. As a result of the lower density of states, quantum capacitance in CNTFET devices becomes comparable to oxide capacitance, which in turn impacts gate capacitance. CNTFET gate capacitance is largely determined by quantum capacitance in the nanometer regime. In sub-threshold region, the capacitance is found to be independent of dielectric and increases exponentially with gate voltage.

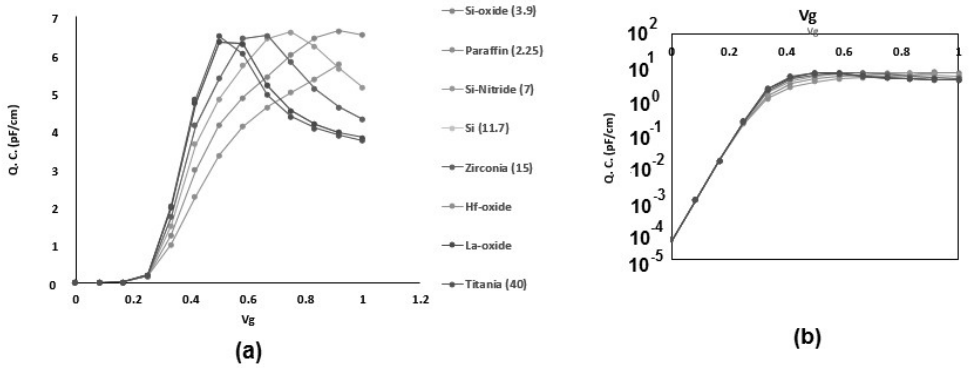

Fig. 5. Variation of quantum capacitance with gate voltage for different gate dielectric materials such as paraffin (2.25), silicon dioxide (3.9), silicon nitride (7), silicon (11.7), zirconia (15), hafnium oxide (25), lanthanum oxide (30) and titania (40) in (a) linear and (b) logarithmic scales

Conclusions

The simulation study that was presented in this paper reveals that CNTFET can be operated in lower voltage and current values, which means that it has the potential to find applications in portable electronic devices. Because current tends to become saturated relatively quickly for high-k materials, the choice of gate dielectric may be contingent on the operating bias range. This is due to the limited supply of electrons in nano-scaled devices. The quantum capacitance limiting factor is also found, where charge decreases as gate voltage increases as a result of the lower density of states.

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